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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,933	03/30/2001	H. Peter Anvin	TRANS52	8288

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,933	ANVIN ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1-3, 5, and 6-9 are objected to because of the following informalities:

Referring to claims 1, 3, and 5, "the fault" referred to in the last line is understood to refer to "the nested fault".

Referring to claim 2, it is not clear if "a level fault handler" is intended to differentiate over "a first level fault handler". For the purpose of examination, "a level fault handler" is understood to refer to "a nested fault handler".

Referring to claims 6-9, "A processor fault handler as claimed..." has no antecedent basis. It is understood to refer to "A fault handler system as claimed..." instead.

Referring to claims 7 and 8, "the storage media" only has antecedence in claim 6. Claim 7 is understood to depend from claim 6 instead.

Referring to claim 9, it is unclear if "fault handling registers" is intended to differentiate over "a first set of fault handling registers". For the purpose of examination, the first instance of "fault handling registers in claim 9 is understood to refer to, instead, "a second set of fault handling registers".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5386563 to Thomas, deceased. Referring to claims 1 and 5, Thomas discloses determining whether a fault is a first level fault (From the abstract, "A data processing apparatus and method are described in which a CPU is operable in either a main processing mode (User32) or an exception processing mode (e.g. FIQ32)."), responding to a determination of a first level fault by saving a first amount of state sufficient to handle a first level fault (From the abstract, "Upon entering the exception processing mode at least one exception data register (R8fiq to R14fiq) is substituted for use in place of a respective corresponding one of the main data registers and the data held within the processing status register is stored within a saved processing status register (SPSRfiq)."), and responding to a determination of a nested fault by saving an additional amount of state before handling the nested fault (From the abstract, "A plurality of exception processing modes are described each having their own associated exception data registers. When a further differing exception occurs within an exception processing mode, the CPU switches to that further differing exception processing mode and uses its own exception data registers and saved processing status register in place of those of the existing processing mode.").

Referring to claim 2, Thomas discloses the step of determining whether a fault is a first level fault comprises storing an indication when a first level fault handler is executed, and determining if an indication has been stored when a nested fault handler is executed (From the abstract, "When a further differing exception occurs within an exception processing mode, the CPU switches to that further differing exception processing mode and uses its own exception data registers and saved processing status register in place of those of the existing processing mode." Further, from line 30 of column 7, "The contents of the CPSR from the User32 mode are saved in the SPSRsvc at step 56 and the contents of the CPSR updated to reflect the SVC32 mode which has been entered at step 58. In particular, the five bit field indicating the processing mode is updated. If, while in the SVC32 mode, a further exception occurs (steps 62) as determined at step 60, such as an aborted memory access, then the Abt32 mode is entered from the SVC32 mode.").

Referring to claim 3, Thomas discloses the steps of executing a first level fault handler after saving a first amount of state sufficient to handle a first level fault (From the abstract, "Upon entering the exception processing mode at least one exception data register (R8fiq to R14fiq) is substituted for use in place of a respective corresponding one of the main data registers and the data held within the processing status register is stored within a saved processing status register (SPSRfiq)."), and executing a different fault handler after saving an additional amount of state before handling the fault (From the abstract, "A plurality of exception processing modes are described each having their own associated exception data registers. When a further differing exception occurs

within an exception processing mode, the CPU switches to that further differing exception processing mode and uses its own exception data registers and saved processing status register in place of those of the existing processing mode.").

Referring to claim 4, Thomas discloses the steps of executing epilogue sequences of instructions after handling any fault handler enabling return of execution to a correct sequence of instructions following a fault last handled (From the abstract, "When the exception processing mode is left, the main data registers are returned for use in place of the exception data registers and the data stored within the saved processing status register is restored to the processing status register.").

Referring to claim 6, Thomas discloses the means for determining whether a fault is a first level fault includes storage media for holding an indication that a processor is handling a fault, and means for detecting the condition of the storage media (From the abstract, "When a further differing exception occurs within an exception processing mode, the CPU switches to that further differing exception processing mode and uses its own exception data registers and saved processing status register in place of those of the existing processing mode." Further, from line 30 of column 7, "The contents of the CPSR from the User32 mode are saved in the SPSRsvc at step 56 and the contents of the CPSR updated to reflect the SVC32 mode which has been entered at step 58. In particular, the five bit field indicating the processing mode is updated. If, while in the SVC32 mode, a further exception occurs (steps 62) as determined at step 60, such as an aborted memory access, then the Abt32 mode is entered from the SVC32 mode.").

Referring to claim 7, Thomas discloses the storage media is a processor register

(from line 30 of column 7, "The contents of the CPSR from the User32 mode are saved in the SPSRsvc at step 56 and the contents of the CPSR updated to reflect the SVC32 mode which has been entered at step 58. In particular, the five bit field indicating the processing mode is updated. If, while in the SVC32 mode, a further exception occurs (steps 62) as determined at step 60, such as an aborted memory access, then the Abt32 mode is entered from the SVC32 mode." Wherein, processing status registers are used.).

Referring to claim 8, Thomas discloses the means for detecting the condition of the storage media includes software running on the processor (See at least figure 4A, wherein routines run on the processor are shown.).

Referring to claim 9, Thomas discloses the means for responding to a determination of a nested fault by saving an additional amount of state before handling the fault includes a second set of fault handling registers in addition to a first set of fault handling registers (From the abstract, "A plurality of exception processing modes are described each having their own associated exception data registers. When a further differing exception occurs within an exception processing mode, the CPU switches to that further differing exception processing mode and uses its own exception data registers and saved processing status register in place of those of the existing processing mode." Further, see figure 2.).

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's History of the Prior Art. Referring to claims 1 and 5, Applicant's History of the Prior Art discloses determining whether a fault is a first level fault (From paragraph

11, "Such hardware is able to handle first level faults since the instruction at which the fault occurred is retained, by the processor but is not capable of handling nested faults by itself."), responding to a determination of a first level fault by saving a first amount of state sufficient to handle a first level fault (From paragraph 11, "the instruction at which the fault occurred is retained".), and responding to a determination of a nested fault by saving an additional amount of state before handling the nested fault (From paragraph 11, "To handle nested faults, such hardware is utilized with software fault handlers which include code for saving and restoring state necessary to handle any level of fault which might occur.").

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 3614740 to Delagi et al.

US 5481719 to Ackerman et al.

US 5588113 to Johnson

US 5944816 to Dutton et al.

US 2001/0047470 to Roche

US 2002/0144099 to Muro, Jr. et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

gc

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SUPERVISORY PATENT EXAMINER
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